What is claimed is:

1. A semiconductor integrated circuit comprising at least three power supply lines and at least two transistors for changing connections to the power supply lines, wherein the first, second and third power supply lines in said power supply lines are placed in said order, and said at least two transistors include first and second transistors respectively placed in the gap between said first and second power supply lines and the gap between said second and third power supply lines formed on the opposite sides of said second power supply line.

2. The semiconductor integrated circuit according to claim 1, wherein at least one of said power supply line is extended in wiring to be connected to an external connection terminal.

3. The semiconductor integrated circuit according to claim 1, further comprising a mutual connection line for connecting together some of said power supply lines having equal potentials, wherein the mutual connection line is not connected to any of said power supply lines other than those having equal potentials.

4. The semiconductor integrated circuit according to claim 1, wherein the area occupied by all of said power supply lines is larger than the area occupied by all of the regions between said power supply lines.

5. The semiconductor integrated circuit according to claim 1, further comprising a gate signal wiring line in order to avoid

a delay of a gate signal propagating through the corresponding one of the gate electrodes of said transistors, the gate signal wiring line having a resistance and a parasitic capacitance lower than those of the gate electrode.

6. The semiconductor integrated circuit according to claim 1, wherein said transistors are thin-film transistors formed on a glass substrate or an insulation substrate other than a semiconductor substrate.

7. A method of manufacturing the semiconductor integrated circuit according to claim 6, comprising advancing crystallization in the gate width direction in a step of crystallizing an amorphous semiconductor layer into a polycrystalline semiconductor.

8. A charge pump circuit comprising the semiconductor integrated circuit according to claim 1, and a configuration of a plurality of capacitors and a plurality of transistors.

9. A layout designing apparatus comprising:

storage means for storing circuit data on a circuit constituted by a plurality of transistors;

search means of searching for a set of routes formed so that passage through any one of the transistors occurs only one time and so that the combination of routes in one set can cover the entire circuit network represented by the circuit data;

extraction means of extracting a set of routes having the smallest number of routes in sets of routes found as search results by said search means;

layout width determination means of determining a layout width from the widths of source and drain electrodes of each transistor, the width of the region between the source and drain electrodes, the width of the region between the source or drain electrodes of some of the adjacent pairs of the transistors not combined into a common electrode, the number of the transistors, and the number of routes contained in the set of routes extracted by said extraction means;

layout determination means of forming information on a layout in which the source, drain, and gate electrodes of the transistors included in said circuit are placed in a small-width region having the width determined by said layout width determination means; and

output means of outputting the layout information determined by said layout determination means.

10. The layout designing apparatus according to claim 9, wherein if the width of the source and drain electrodes of each transistor is Wi; the width of the region between the source and drain electrodes is Lj; the width of the region between the source or drain electrodes of some of the adjacent pair of transistors not combined into a common electrode is Pk; the number of the transistors is n; and the number of routes included in the set of routes extracted by said extraction means is m, said width

determination means determines a value given by the following expression as the layout width:

$$\sum_{i=1}^{n+m} Wi + \sum_{j=1}^{n} Lj + \sum_{k=1}^{m-1} Pk$$

11. The layout designing apparatus according to claim 9, wherein the width of the region between the source or drain electrodes of some of the adjacent pair of transistors not combined into a common electrode is smaller than the width of the region between the source and drain electrodes.

12. The layout designing apparatus according to claim 9, wherein said layout determination means alternately places the source/drain electrodes and the gate electrodes in correspondence with each of the routes in an arbitrary one of the at least one set of routes extracted by said extraction means in the order of passage through the transistors designated with the route or in the order reverse to the passage order.

13. The layout designing apparatus according to claim 9, further comprising mutual wiring length shortest set determination means of determining a set of routes having the shortest entire length of mutual wiring for connecting together some of the source or drain electrodes having equal potentials in the at least one set of routes extracted by said extraction means, the order of the plurality of routes contained in the set of routes, and the direction in which each route contained in the set is connected, wherein said layout determination means alternately places the

source/drain electrodes and the gate electrodes in accordance with the set of routes, the order of the plurality of routes contained in the set of routes and the connection direction of each route determined by said mutual wiring length shortest set determination means.

14. The layout designing apparatus according to claim 12, wherein said layout determination means determines the placement of a mutual connection line which connects together some of the source or drain electrodes having equal potentials.

15. The layout designing apparatus according to claim 12, wherein said layout determination means extends, for connection to an external terminal, the length of at least one of the source and drain electrodes designated as an electrode to be connected to the external terminal according to the circuit data.

16. A semiconductor integrated circuit comprising a structure in which source, drain and gate electrodes of transistors included in a circuit are placed in a small-width region having a width determined from the number of routes in a set of routes having the smallest number of routes in sets of routes formed so that passage through any one of the transistors included in the circuit occurs only one time and so that the combination of routes in one set can cover the entire circuit network of the circuit, determined from the widths of source and drain electrodes of each transistor, determined from the width of the region between the source and drain electrodes, determined from the width of

the region between the source or drain electrodes of some of the adjacent pairs of the transistors not combined into a common electrode, and determined from the number of the transistors included in the circuit.

17. The semiconductor integrated circuit according to claim 16, wherein if the width of the source and drain electrodes of each transistor is Wi; the width of the region between the source and drain electrodes is Lj; the width of the region between the source or drain electrodes of some of the adjacent pair of transistors not combined into a common electrode is Pk; the number of the transistors is n; and the number of routes included in the set of routes having the smallest number of routes is m, said small-width region has a width expressed by the following expression:

$$\sum_{i=1}^{n+m} Wi + \sum_{j=1}^{n} Lj + \sum_{k=1}^{m-1} Pk$$

18. The semiconductor integrated circuit according to claim 16, wherein the width of the region between the source or drain electrodes of some of the adjacent pair of transistors not combined into a common electrode is smaller than the width of the region between the source and drain electrodes.

19. The semiconductor integrated circuit according to claim 16, wherein the source/drain electrodes and the gate electrodes are alternately placed in correspondence with each of the routes in an arbitrary one of the at least one set of routes having

the smallest number of routes in the order of passage through the transistors designated with the route or in the order reverse to the passage order.

20. The semiconductor integrated circuit according to claim 16, wherein the source/drain electrodes and the gate electrodes are alternately placed in accordance with a set of routes having the shortest entire length of mutual wiring for connecting together some of the source or drain electrodes having equal potentials in the sets of routes having the smallest number of routes, in accordance with the order of the plurality of routes contained in the set of routes, and in accordance with the connection direction of each route and the connection direction of each route contained in the set of route.

21. The semiconductor integrated circuit according to claim 19, wherein some of the source or drain electrodes having equal potentials are connected to each other by a mutual connection line which extends across the source or drain electrodes.

22. The semiconductor integrated circuit according to claim 19, wherein at least one of the source and drain electrodes of the transistors to be connected to an external terminal is extended for connection to the external terminal.

23. The semiconductor integrated circuit according to claim 16, wherein said transistors are thin-film transistors formed

on a glass substrate or an insulation substrate other than a semiconductor substrate.

24. A method of manufacturing the semiconductor integrated circuit according to claim 23, comprising advancing crystallization in the gate width direction in a step of crystallizing an amorphous semiconductor layer into a polycrystalline semiconductor.

25. A program for enabling a computer having storage means for storing circuit data on a circuit constituted by a plurality of transistors to operate, comprising:

step of searching for a set of routes formed so that passage through any one of the transistors occurs only one time and so that the combination of routes in one set can cover the entire circuit network represented by the circuit data;

step of extracting a set of routes having the smallest number of routes in sets of routes found as search results by said step of searching for a set of routes;

step of determining a layout width from the widths of source and drain electrodes of each transistor, the width of the region between the source and drain electrodes, the width of the region between the source or drain electrodes of some of the adjacent pairs of the transistors not combined into a common electrode, the number of the transistors, and the number of routes contained in the set of routes extracted by said step of extraction a set of routes;

step of forming information on a layout in which the source, drain, and gate electrodes of the transistors included in said circuit are placed in a small-width region having the width determined by said step of determining a layout width; and

step of outputting the layout information determined by said step of forming information on a layout.

26. The program according to claim 25, wherein if the width of the source and drain electrodes of each transistor is Wi; the width of the region between the source and drain electrodes is Lj; the width of the region between the source or drain electrodes of some of the adjacent pair of transistors not combined into a common electrode is Pk; the number of the transistors is n; and the number of routes included in the set of routes extracted by said extraction means is m, said step of determining a layout width determines a value given by the following expression as the layout width:

$$\sum_{i=1}^{n+m} Wi + \sum_{j=1}^{n} Lj + \sum_{k=1}^{m-1} Pk$$

27. The program according to claim 25, wherein the width of the region between the source or drain electrodes of some of the adjacent pair of transistors not combined into a common electrode is smaller than the width of the region between the source and drain electrodes.

28. The program according to claim 25, wherein said step of forming information on a layout alternately places the

source/drain electrodes and the gate electrodes in correspondence with each of the routes in an arbitrary one of the at least one set of routes extracted by said step of extracting a set of routes in the order of passage through the transistors designated with the route or in the order reverse to the passage order.

29. The program according to claim 25, further comprising making the computer function as step of determining a set of routes having the shortest entire length of mutual wiring for connecting together some of the source or drain electrodes having equal potentials in the at least one set of routes extracted by said step of extracting a set of routes, the order of the plurality of routes contained in the set of routes, and the direction in which each route contained in the set is connected, wherein said step of forming information on a layout alternately places the source/drain electrodes and the gate electrodes in accordance with the set of routes, the order of the plurality of routes contained in the set of routes and the connection direction of each route determined by said step of determining a set of routes.

30. A Layout designing method of a semiconductor integrated circuit, comprising:

step of searching for a set of routes formed so that passage through any one of the transistors occurs only one time and so that the combination of routes in one set can cover the entire circuit network represented by the circuit data;

step of extracting a set of routes having the smallest number of routes in sets of routes found as search results by said step of searching for a set of routes;

step of determining a layout width from the widths of source and drain electrodes of each transistor, the width of the region between the source and drain electrodes, the width of the region between the source or drain electrodes of some of the adjacent pairs of the transistors not combined into a common electrode, the number of the transistors, and the number of routes contained in the set of routes extracted by said step of extraction a set of routes;

step of forming information on a layout in which the source, drain, and gate electrodes of the transistors included in said circuit are placed in a small-width region having the width determined by said step of determining a layout width; and

step of outputting the layout information determined by said step of forming information on a layout.